REMARKS

This Response responds to the Office Action dated August 1, 2005 in which the Examiner rejected claim 1 under 35 U.S.C. §102(e) and objected to claims 2-17 as being dependent upon a rejected base claim but would be allowable if rewritten in independent form.

Applicants respectfully point out that claims 1-17 are pending in the application and not claims 1-27 as indicated on PTO-326.

Claim 1 claims a semiconductor integrated circuit comprising first and second terminals, a voltage generating circuit, an internal circuit and a A/D conversion circuit. The first terminal receives an external power supply voltage provided from outside. The voltage generating circuit lowers the external power supply voltage and generates an internal voltage. The internal circuit uses the internal voltage. The A/D conversion circuit converts the internal voltage from an analog value to a digital value so as to output a digital signal to the outside. The second terminal provides the digital signal to the outside.

Through the structure of the claimed invention having an internal circuit and A/D conversion circuit use an internal voltage from a voltage generating circuit, as claimed in claim 1, the claimed invention provides a semiconductor integrated circuit in which an output voltage can be observed as a digital value which facilitates measurement. The prior art does not show, teach or suggest the invention as claimed in claim 1.

Claim 1 was rejected under 35 U.S.C. §102(e) as being anticipated by *Kanke et al.* (U.S. Patent No. 6,839,643).

Kanke et al. appears to disclose a sensor circuit 1 is connected to a power supply 10 to heat a heating resistor 11 to a constant temperature, and forms a sensing part of a thermal type flowmeter that measures a flow rate running through the heating resistor 11 by the interchange of heats generated according to the flow velocity. A digital error regulation unit 2 composed of digital means including a microcomputer and dedicated logics receives an output signal Vin from the sensor circuit 1. The signal Vin is converted into a digital value by an A/D converter 21. An arithmetic circuit 22 applies an error correction to the digital value according to the correction data provided in a rewritable memory 23. A D/A converter 24 outputs to an engine control unit 5 a voltage value that is equal to the output signal Vin from the sensor circuit 1. The sensor circuit 1, the digital error regulation unit 2, and a power supply circuit 3 to generate a reference voltage constitute a flow rate measuring device 4. In the engine control unit 5, an A/D converter 51 converts an output signal Vout from the flow rate measuring device 4 into a digital value, and the digital value is used for the engine control. (col. 4, lines 46-67)

Thus, *Kanke et al.* merely discloses a power supply circuit 3 which generates a reference voltage and a sensor circuit 1 outputting Vin. Nothing in *Kanke et al.* shows, teaches or suggests both an internal circuit and an A/D conversion circuit receiving the internal voltage as claimed in claim 1. Rather *Kanke et al.* merely discloses A/D converter receives Vin while sensor circuit 1 receives Vref.

Additionally, *Kanke et al.* merely discloses a flow rate measuring device 4 and an engine control unit 5. Nothing in *Kanke et al.* shows, teaches or suggests a semiconductor integrated circuit including first and second terminals, a voltage generating circuit, an internal circuit and an A/D conversion circuit and outputting a

digital signal to the outside as claimed in claim 1. Rather, *Kanke et al.* does not disclose a semiconductor integrated circuit, nor does *Kanke et al.* output a signal outside, but only outputs out to engine control unit 5.

Since nothing in *Kanke et al.* shows, teaches or suggests the structure as claimed in claim 1, Applicants respectfully request the Examiner withdraws the rejection to claim 1 under 35 U.S.C. §102(e).

Since objected to claims 2-17 depend from an allowable claim, Applicants respectfully request the Examiner withdraws the objection thereto.

The prior art of record, which is not relied upon, is acknowledged. The references taken singularly or in combination do not anticipate or make obvious the claimed invention.

Thus it now appears that the application is in condition for reconsideration and allowance. Reconsideration and allowance at an early date are respectfully requested.

If for any reason the Examiner feels that the application is not now in condition for allowance, the Examiner is requested to contact, by telephone, the Applicants' undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this case.

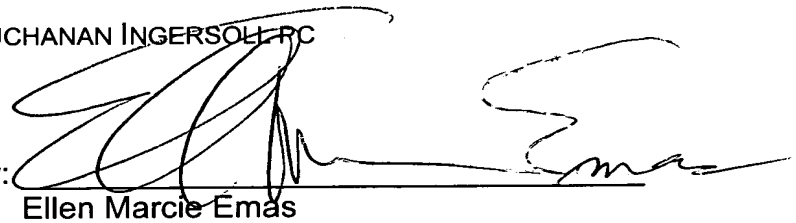
In the event that this paper is not timely filed within the currently set shortened statutory period, Applicants respectfully petition for an appropriate extension of time. The fees for such extension of time may be charged to our Deposit Account No. 02-4800.

In the event that any additional fees are due with this paper, please charge our Deposit Account No. 02-4800.

Respectfully submitted,

BUCHANAN INGERSOLL PC

Date: November 1, 2005

By: 

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